**Research and Development Technical Report**

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# HIGH CAPACITANCE THIN-FILM STRUCTURES

## FINAL REPORT

*By*

M. S. WASSERMAN — A. E. FEUERSANGER

**September 1972**

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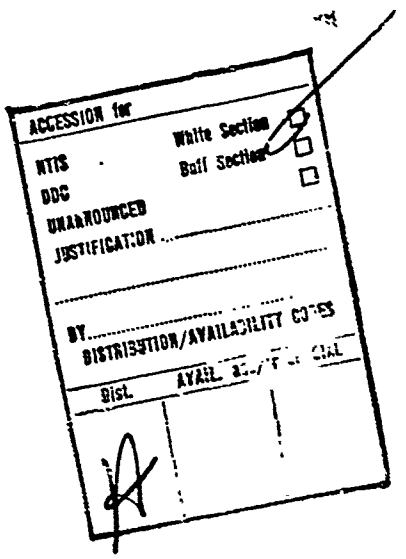

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## ABSTRACT

Silicon integrated square-wave oscillator circuits with an output frequency of 2 to 3.5 kHz were fabricated with thin-film Al-$Al_2O_3$-NiO-Al capacitors on their surface as the frequency-determining components. The capacitor values were in the range of 0.4 to 1.8 nF, corresponding to a specific capacitance between 3 and 10 $\mu F/in^2$. Minor modifications of the fabrication process are proposed for improving the uniformity of the capacitance values and maintaining the design goal of 10 $\mu F/in^2$.

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# 1. INTRODUCTION

This is the Final Report on a program whose general objective is to advance the state-of-the-art in integrated circuit technology by demonstrating the ability to incorporate relatively high value thin-film capacitors into integrated circuits. The specific objective is to utilize the charge storage capability of the barrier layer that resides at the interface between a reactively sputtered nickel oxide film and an aluminum film to achieve a specific capacitance of 10 $\mu F/in^2$ (0.9 $pF/mil^2$). Furthermore, it is required to develop a fabrication procedure for these capacitors that is compatible with silicon monolithic circuit processing and to deliver complete circuits as test vehicles. The circuit selected was a square-wave oscillator that requires two capacitors of 0.001 $\mu F$ or greater. The desired operating characteristics include a frequency between 0.9 and 1.2 kHz and a square-wave output with a voltage excursion from less than 1 volt to more than 7 volts when a 9-volt power supply is used.

The essentials of a deposition method for the 10 $\mu F/in^2$ thin-film capacitors were developed in the first phase of this program.[1] During the second phase[2] progress was made toward development of a method for incorporating the capacitors in silicon integrated circuits. The result was the fabrication of a 10-kHz oscillator chip with a 0.003-$\mu F$ capacitor. The most recent phase, which is described in this report, was devoted to the refinement of the integrated circuit fabrication process, with the goal of making the square-wave oscillator for the 0.9 to 1.2 kHz range. A 60 mil x 70 mil chip that contains a 0.001-$\mu F$ and a 0.0018-$\mu F$ capacitor was designed and fabricated. Although the process that was finally developed provided a 60 to 80 percent yield of operating oscillator circuits, it introduced problems of control over the capacitance values, with the result that the majority of the delivered circuits operate in the 2 to 3 kHz range. In spite of this difficulty, a sufficient number of 10 $\mu F/in^2$ capacitors have been incorporated into silicon integrated circuits to demonstrate that the approach developed under this program can lead, after minor modifications, to a viable fabrication technique.

## 2. FABRICATION AND PROPERTIES OF THE THIN-FILM CAPACITOR

### 2.1 Fabrication of the Basic Capacitor

The thin-film capacitor shown in cross section in Figure 1 is fabricated in four steps that include evaporation of the aluminum base electrode, thermal oxidation of the aluminum, reactive sputtering of nickel in pure oxygen, and evaporation of the aluminum top electrode. The thermal oxidation step is a critical one, since it forms the capacitor dielectric, which is an $Al_2O_3$ film less than 100 Å thick. The relationship between the $Al_2O_3$ film thickness and the oxidation time is shown in Figure 2. The effect of the aluminum thickness on the oxidation rate is a reproducible one which has not been explained. There may be a change in grain size or surface roughness during the aluminum deposition that affects the oxidation rate. The capacitors are usually formed by oxidizing a 1 $\mu$m aluminum film in dry oxygen at 500°C for three minutes. The nickel oxide film, which is approximately 1000 Å thick, is formed by dc sputtering of nickel for 15 minutes at 50-millitorr oxygen pressure and a cathode potential of 2.5 kV. The auxiliary steps required for incorporating the capacitor in an integrated circuit are described in Section 3.2.2.

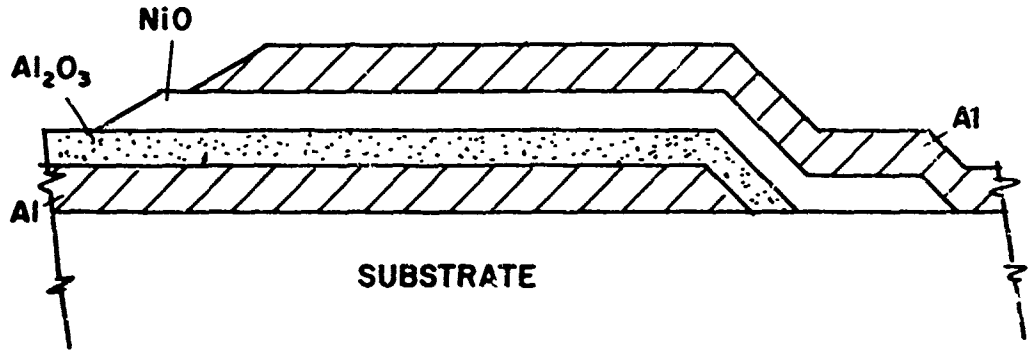



Figure 1. Cross Section of 10 $\mu F/in^2$ Thin-Film Capacitor.

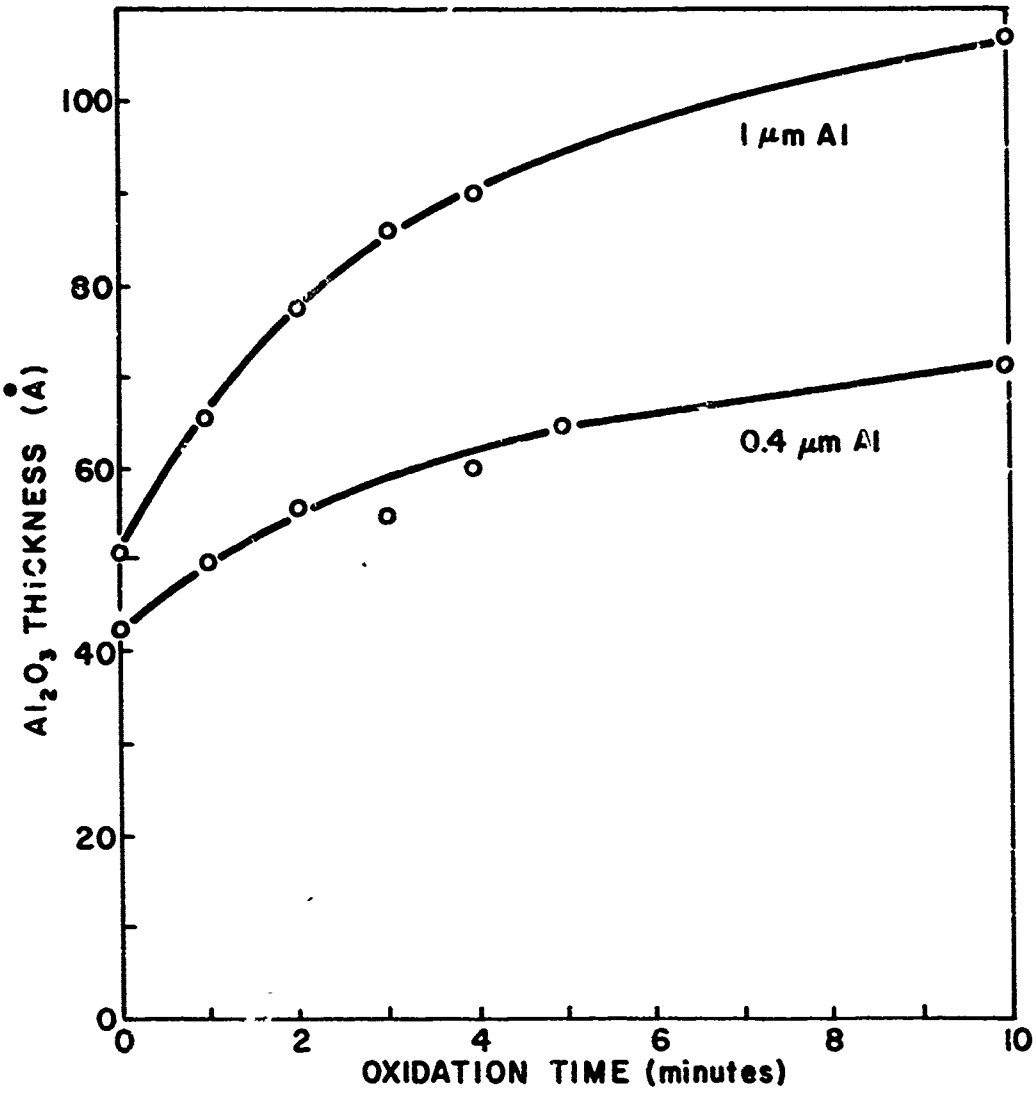



Figure 2. Thermal Oxidation Rate of Aluminum at 500°C.

## 2.2 AC Properties

A typical 100 $mil^2$ capacitor has a value of 0.8 to 1 nF and a dissipation factor of 0.015 to 0.032 at 1 kHz. Measurements of the frequency dependence and temperature dependence of the capacitance and dissipation factor are summarized in Figures 3 through 6. Experimental results are shown for four samples in which the NiO thickness decreases from A to C, and is zero in Sample D. The ac properties, and particularly the temperature dependence, are qualitatively in agreement with a model involving potential barriers at one or both of the metal-oxide interfaces. In the model, the capacitor is represented by the equivalent network shown in Figure 7(a), where the interface regions and the NiO film are each represented by a resistor and capacitor in parallel. In this model the barrier capacitance $C_C$ (or $C_A$) is much greater than the NiO capacitance $C_B$ because the barrier thickness is much less than that of the NiO film. The simplified network in Figure 7(b) is obtained by combining the two barrier capacities into $C_D$. In most of the discussion it is assumed that the only effective barrier is a thin $Al_2O_3$ film at the interface between the NiO and the Al base electrode. The simplified network in Figure 7(b) leads to the following equations for the equivalent series capacitance and the dissipation factor:

$$C_s = \left[ \frac{\omega^2 R_D^2 C_D}{1 + \omega^2 R_D^2 C_D^2} + \frac{\omega^2 R_B^2 C_B}{1 + \omega^2 R_B^2 C_B^2} \right]^{-1} \tag{1}$$

and

$$D = \frac{R_D\left(1+\omega^2 R_B^2 C_B^2\right) + R_B\left(1+\omega^2 R_D^2 C_D^2\right)}{\omega R_D^2 C_D\left(1+\omega^2 R_B^2 C_B^2\right) + \omega R_B^2 C_B\left(1+\omega^2 R_D^2 C_D^2\right)} \tag{2}$$

where the subscript B refers to the NiO film and the subscript D refers to the $Al_2O_3$ film.

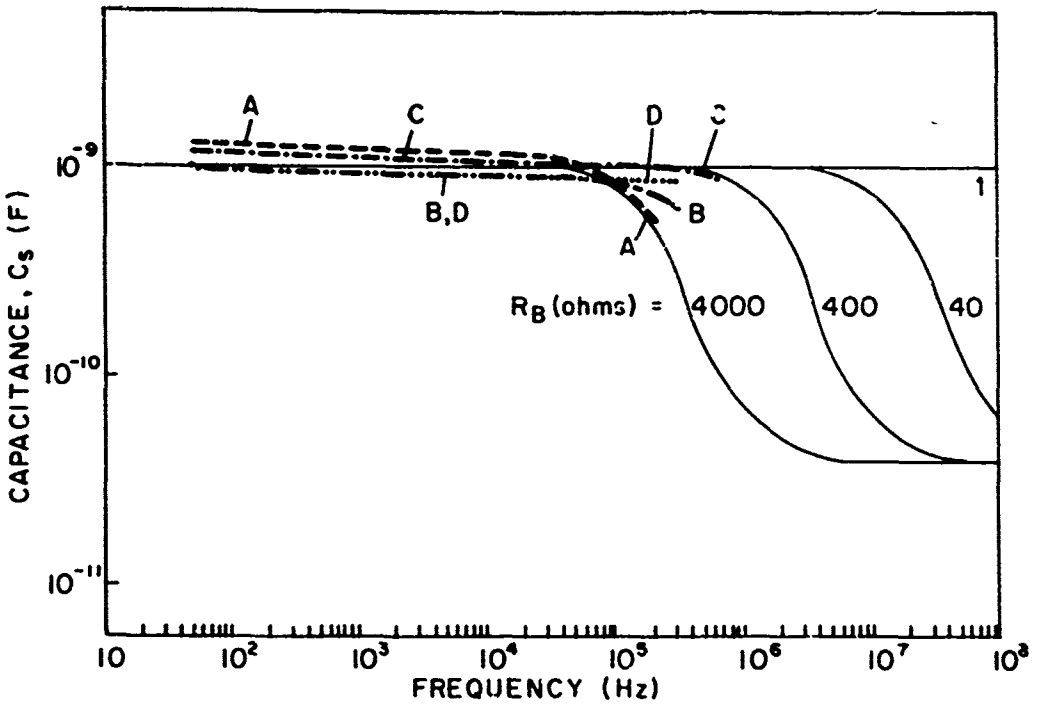



**Figure 3.** Experimental and Calculated Frequency Dependence of Capacitance. Values of $R_B$ and $R_D$ ($10^8$ ohms) chosen for a 100 $mil^2$ capacitor. NiO thickness decreases from Sample A to Sample C. Sample D has no NiO.

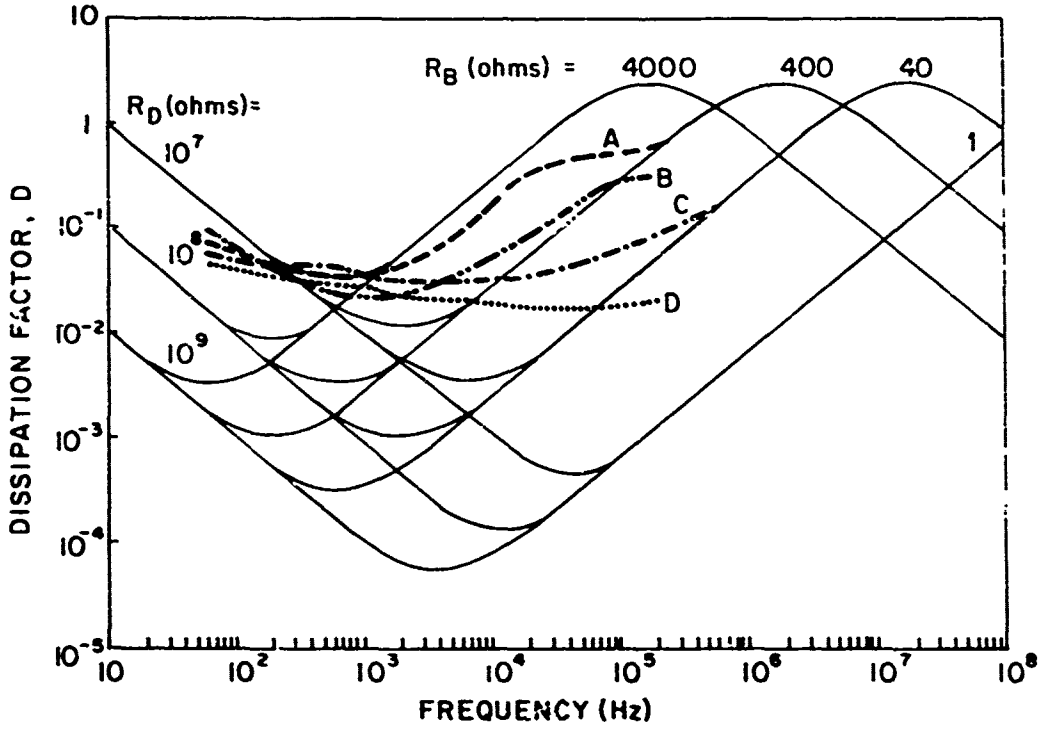



**Figure 4.** Experimental and Calculated Frequency Dependence of Dissipation Factor. (Same samples as in Figure 3.)

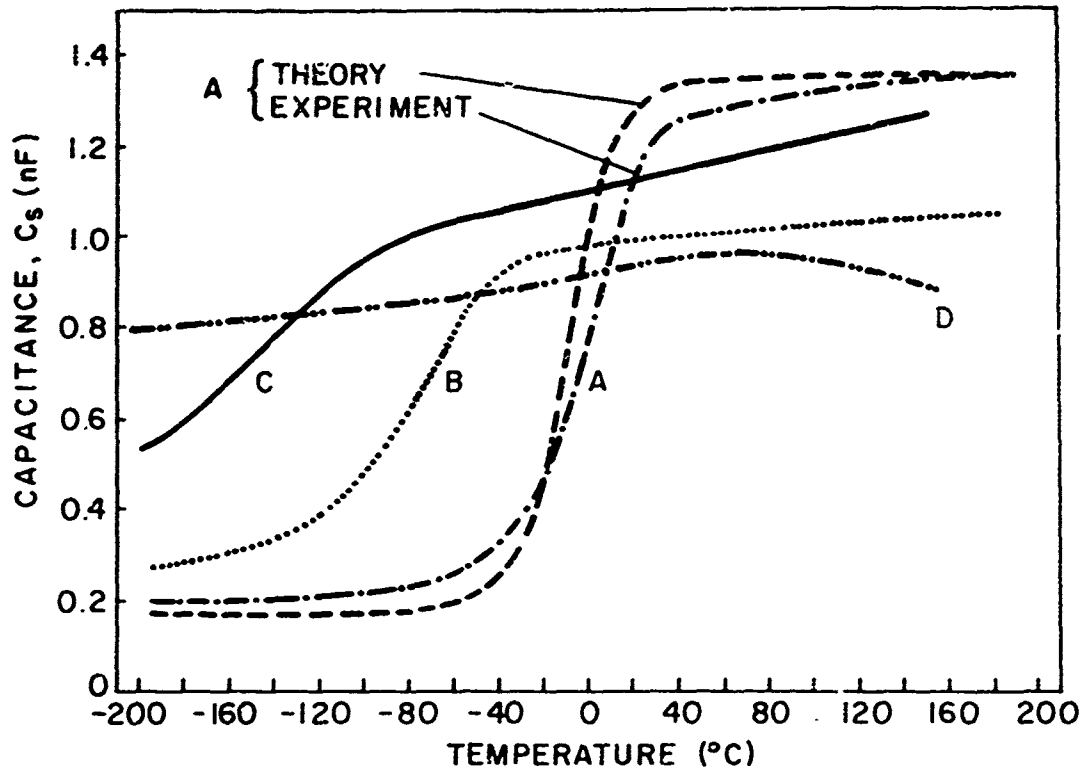



Figure 5. Experimental Temperature Dependence of Capacitance for Different NiO Thicknesses. Also shown in the calculated curve for Sample A.

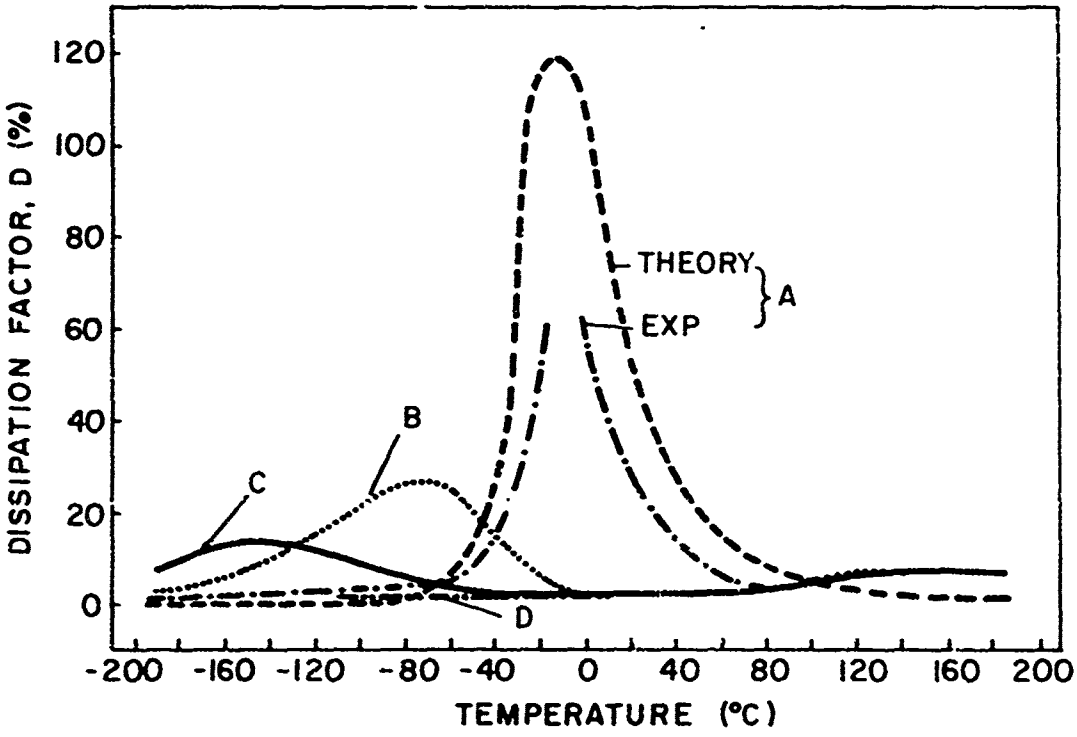
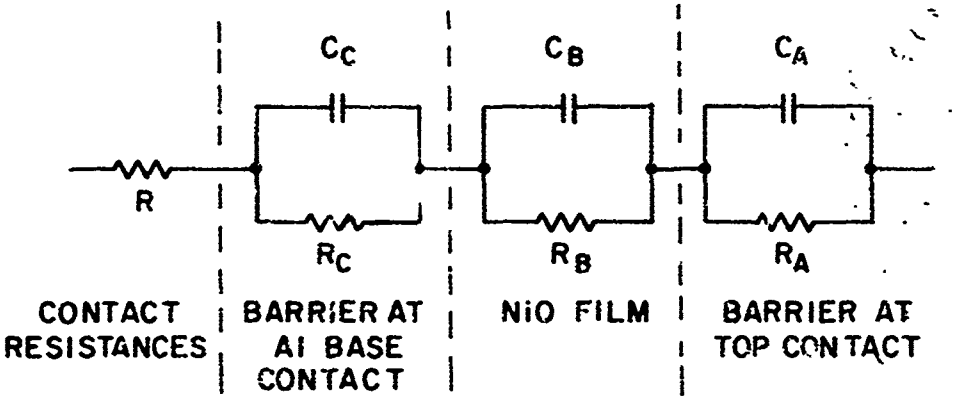
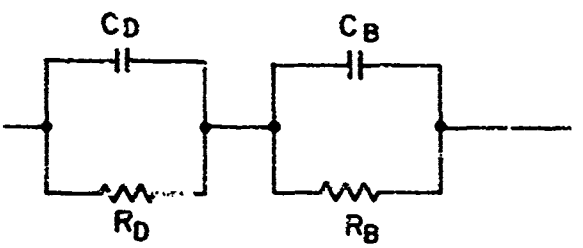



Figure 6. Temperature Dependence of Dissipation Factor for the Same Samples Shown in Figure 3.




(a) COMPLETE NETWORK




(b) SIMPLIFIED NETWORK

Figure 7. Equivalent Network for Thin-Film Capacitor.

The calculated curves in Figures 3 and 4 were derived for reasonable values of $R_D$ and $R_B$. For example, a four-point probe resistivity measurement[1] of a 1500 Å NiO film yields a value of 4000 ohms for $R_B$. The order of the calculated curves is consistent with the variation in NiO thickness in both figures. The lack of agreement between the observed and calculated dissipation factors indicates that the capacitors possess a frequency-independent loss mechanism that is not included in the model. The equivalent series resistance calculated from the high-frequency dissipation factor is essentially the same as the dc resistance of the NiO film.

The temperature dependence of the capacitance and dissipation factor was obtained by assuming the NiO to be a semiconductor whose resistance is a simple exponential function of temperature:

$$R_B = A \exp(E/2kT) \tag{3}$$

reflecting a single activation energy E. Combining Eq. (3) with Eqs. (1) and with (2), and assuming $R_D$ to be very large results in

$$C_S = C_D\left(\frac{1 + \omega^2 C_B^2 A^2 \exp(E/kT)}{1 + \alpha\,\omega^2 C_B^2 A^2 \exp(E/kT)}\right) \tag{4}$$

and

$$D = \frac{(\alpha - 1)\,\omega C_B A \exp(E/2kT)}{1 + \alpha\,\omega^2 C_B^2 A^2 \exp(E/kT)} \tag{5}$$

where $\alpha = 1 + C_D/C_B$.

The high-temperature limit of $C_S$ is $C_D$, the $Al_2O_3$ capacitance, and the low-temperature limit is the series combination of $C_D$ and $D_B$. The dissipation factor is low in the two limits, and exhibits a maximum at the temperature of transition from high to low capacitance. It was predicted from this model that the transition temperature will

be shifted to lower values as the NiO thickness is reduced. The confirmation is shown in Figures 5 and 6, which give $C_S$ and D as a function of temperature for the three samples with different NiO thicknesses and for the one sample with no NiO. Also shown are the calculated curves for Sample A, which were fitted by using the experimental values of capacitance at the two temperature limits and the values 0.5 ohm and 0.6 eV for the coefficient and the activation energy in Eq. (3). The high-temperature capacitance in Figure 5 is that of the $Al_2O_3$ film; its variability reflects the fact that $Al_2O_3$ films were prepared under different conditions. More significant is the fact that the low-temperature capacitance is an inverse function of the NiO thickness, as predicted from Eq. (4), and the transition temperature varies in direct relation to the thickness. Sample D contains no NiO, and therfore shows no transition. In all samples the temperature dependence of the capacitance at high temperatures is approximately that of the $Al_2O_3$ film. In addition to providing confirmation of the model, Figure 5 demonstrates the practical result that capacitors can be fabricated with a small linear change in capacitance over the temperature range of -80° to +150°C.

The dissipation data in Figure 6 also confirm the model. The $Al_2O_3$ film shows no maximum, and the maximum in the other samples shifts to lower temperature as the NiO thickness is reduced. The decrease in the value of $D_{max}$ with decreasing NiO thickness is explained by differentiating Eq. (5) with respect to temperature and equating to zero. This yields

$$D_{max} = \frac{\alpha - 1}{2\alpha^{1/2}} \tag{6}$$

which is a direct function of $C_D/C_B$ only. A quantitative discrepancy appears in the magnitude of $D_{max}$ for curves B and C. Whereas the experimental values are less than 0.3, the calculated values are approximately 0.9 and 0.6, respectively.

## 2.3 DC Properties

Typical dc current-voltage curves for 100-$mil^2$ test capacitors are shown in Figure 8. Curves are shown for three capacitors on a test wafer that contained 64 elements.

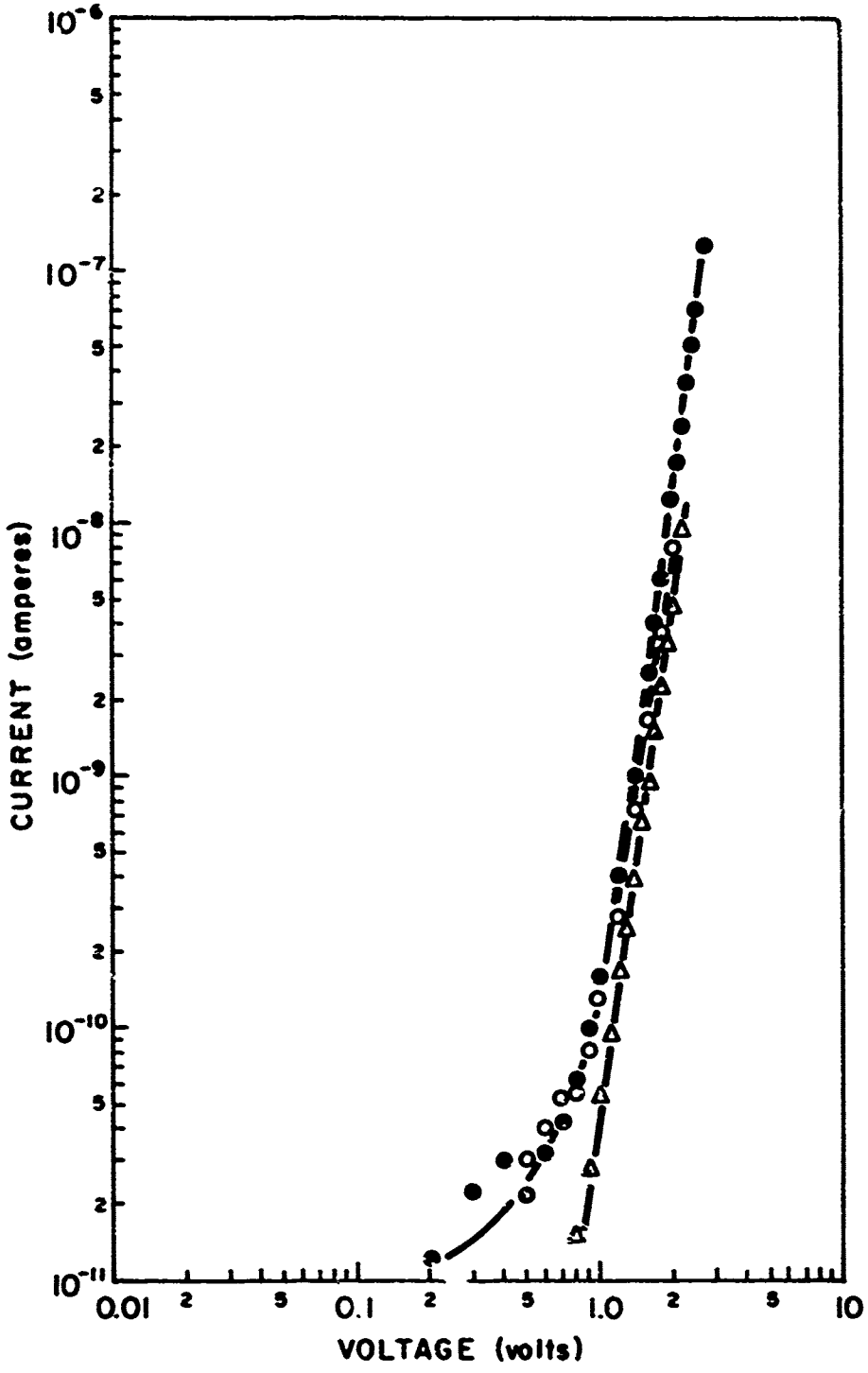



Figure 8. Current-Voltage Characteristics for 100-Mil$^2$ Capacitors With Aluminum Top Electrode.

For potentials up to about 1 volt, the insulation resistance is greater than 10,000 megohms. Since the thickness of the $Al_2O_3$ film, determined both by ellipsometry and from the capacitance, is less than 100 Å, it is to be expected that quantum mechanical tunneling will contribute to the current-voltage characteristic. Indeed, the experimental curves fit a tunneling model reasonably well, especially at very low voltage.[2] Near 1 volt, a Frenkel-Poole conduction mechanism gives a better fit.[2]

The ability of the capacitor to operate near 5 volts without breakdown is attributable to the presence of the semiconductor film. This is demonstrated by the fact that $Al_2O_3$ films of comparable capacitance break down near 1 volt, and often contain initial shorts, when the NiO film is not present. According to our present working hypothesis, the NiO-$Al_2O_3$-Al structure is analogous to the solid tantalum electrolytic capacitor with the $MnO_2$-$Ta_2O_5$-Ta structure. Accordingly, the function of the NiO is to act as an oxidizer for the aluminum, thereby healing any pinholes that might exist after fabrication or that tend to form during operation. If this view of the role of the semiconductor in the breakdown mechanism is correct, then a criterion for the selection of the semiconductor is that the driving force for oxidation of aluminum in the presence of the semiconductor be as large as possible. In other words, the oxidation potential of the oxide semiconductor should be high. By this criterion, both $PbO_2$ and $MnO_2$ are far superior to NiO. Furthermore, the first two tend to form the divalent ion when they react with aluminum, whereas NiO probably forms metallic nickel, which would increase the probability of leaving a conductive path in incipient pinholes after reaction with the aluminum.

Still another advantage of $PbO_2$ and $MnO_2$ is that their resistivity is considerably lower than that of NiO. The high-frequency dissipation of the resulting capacitor would therefore be lower as a result of the lower series resistance.

## 2.4 Operational Tests

The thin-film capacitors have displayed excellent stability in a $10^4$-hour life test. Twenty 100-$mil^2$ capacitors were connected in parallel and operated in a discrete version of the square-wave oscillator described in Section 3.1. They were subjected to a 2.5-volt triangular waveform similar to that shown in Figure 11. The initial total capacitance was

17.10 nF, and the dissipation factor was 0.031 at 1 kHz. After 10,130 hours of continuous operation in the ambient, the capacitance was 16.98 nF, a decrease of 0.7 percent, and the dissipation factor was 0.041.

Four test capacitors were subjected to screening tests as prescribed in Mil-Std-883, procedure method 5004, Class B. The samples had a specific capacitance of 7 $pF/mil^2$ and dissipation factors between 0.02 and 0.03. The tests included:

(1) Stabilization bake, Method 1008 (24 hours at 150°C).

(2) Temperature cycling, Method 1010 (10 cycles between -65°C and 150°C).

(3) Burn-in test, Method 1015 (168 hours at 125°C under operational bias).

The samples were essentially unaffected by the first two tests, as shown in the following table:

| | $\frac{\Delta C}{C}$ | $\frac{\Delta D}{D}$ |
|---|---|---|
| Stabilization bake | +0.002 | -0.0035 |
| Temperature cycling | -0.0006 | -0.016 |

These values represent the average of the four samples; there was little variation among the four. When the burn-in test was performed with the capacitors connected in the square-wave oscillator circuit, two samples broke down under bias at 125°C. The remaining two were operated at 105°C for 168 hours with resulting values of $\Delta C/C = +0.041$ and $\Delta D/D = +0.27$.

## 3. INTEGRATED CIRCUITS INCORPORATING THE THIN-FILM CAPACITORS

This program was directed toward the realization of monolithic silicon circuits containing the thin-film Al-$Al_2O_3$-NiO-Al capacitors on the surface of the silicon. Although hybrid circuits are also of interest, it was decided that a solution to the more difficult problems of materials and processing compatibility inherent in the monolithic circuits would be of greater value, and that it would simplify later work on hybrid circuits.

## 3.1 Preliminary Results

Since the earliest capacitors were formed simply by evaporation and sputtering of the component films through masks, it was necessary to develop photolithographic etching techniques for use in the integrated circuit fabrication. The nickel oxide is etched in 85 percent sulfuric acid at 50°C, using Dynachem CMR 5000 photoresist. Sufficient resolution is achieved, and the underlying oxidized aluminum is not attacked rapidly. The aluminum is removed without attacking the NiO by phosphoric acid at 70°C using Shipley AZ 1350 photoresist.

The first circuit chosen to test the fabrication process[2] was a simple emitter-coupled square-wave oscillator shown schematically in Figure 9. The capacitor is charged and discharged through constant-current sources determined by the component pairs $Q_3, R_4$ and $Q_4, R_6$. The resulting triangular-waveform voltage appearing across the capacitor is shown in the diagram. The frequency of the square-wave output is proportional to the current divided by the capacitance. The circuit was first shown to operate properly in breadboard form, using both conventional capacitors and discrete thin-film capacitors prepared during the initial phase of the program. In fact, the extended life test discussed in Section 2.4 uses the breadboard version of the oscillator circuit to evaluate the sample capacitors.

The resistors and transistors in the integrated version are located on a dielectrically isolated general-purpose chip (Figure 10) which is fabricated routinely in our Laboratories. It is designed with a sufficient number of transistors, resistors, and bus-bars to permit the implementation of a wide variety of circuits by fabricating a single interconnection mask. Those components used in the oscillator are identified in Figure 10 with the symbols used in the schematic. The areas $C_1$, $C_2$, and $C_3$ are used for the thin-film capacitors. Their total area is sufficient to form a capacitor of approximately 0.003 $\mu$F (10 $\mu F/in^2$) by parallel connection, with a resulting output frequency near 10 kHz. The dielectric isolation feature of the chip is a convenience, but it is not a necessity for incorporating the thin-film components. The voltage waveforms in Figure 11 were obtained from a circuit with a 0.0027 $\mu$F capacitor and an output frequency of 11.1 kHz. The applied voltages were: $V_1 = +2.2$ volts, $V_2 = +3.3$ volts, $V_3 = -2.2$ volts. The following sequence of steps was employed in fabricating the oscillator:

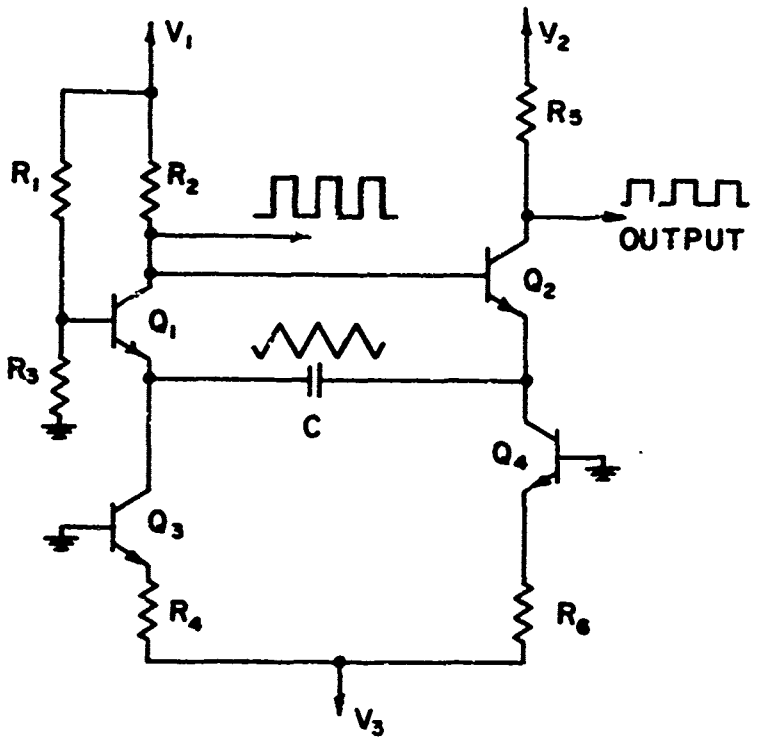



Figure 9. Emitter-Coupled Square-Wave Oscillator Circuit Using a Thin-Film Capacitor.

The transistors and resistors contained in the circuit chip (Figure 10) have the following values:

$Q_1$ to $Q_4$ are transistors similar to the 2N2218

$R_1$ = 5.3 kilohms

$R_2$ = 8.5 kilohms

$R_3$ = 1.2 kilohms

$R_4$ = 10.2 kilohms

$R_5$ = 4.0 kilohms

$R_6$ = 10.4 kilohms

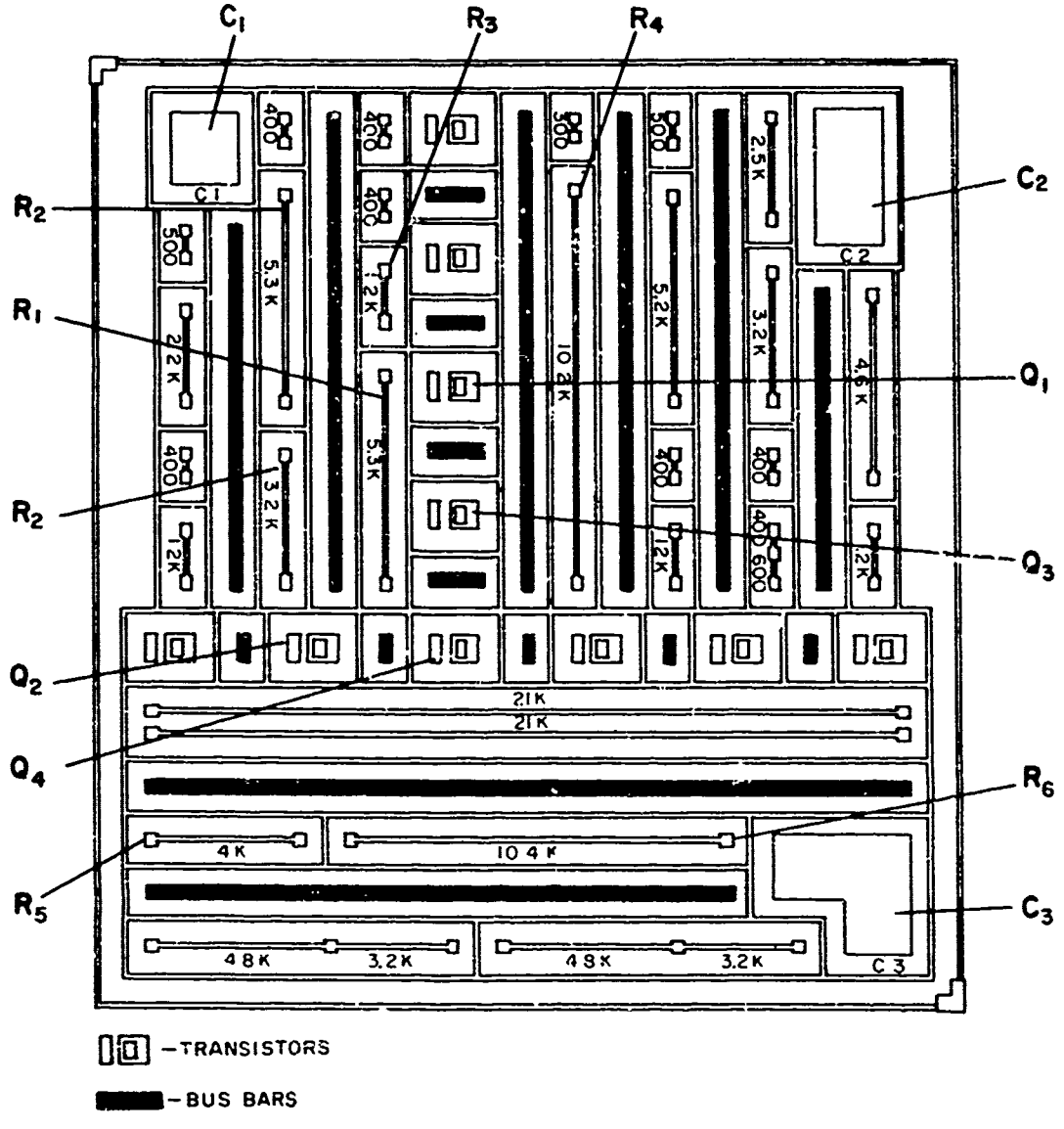



Figure 10. Topography of Dielectrically Isolated Silicon "Breadboard Chip". The dimensions of the chip are 0.122 x 0.126 inch. The locations of the components used in the integrated square-wave oscillator are indicated.

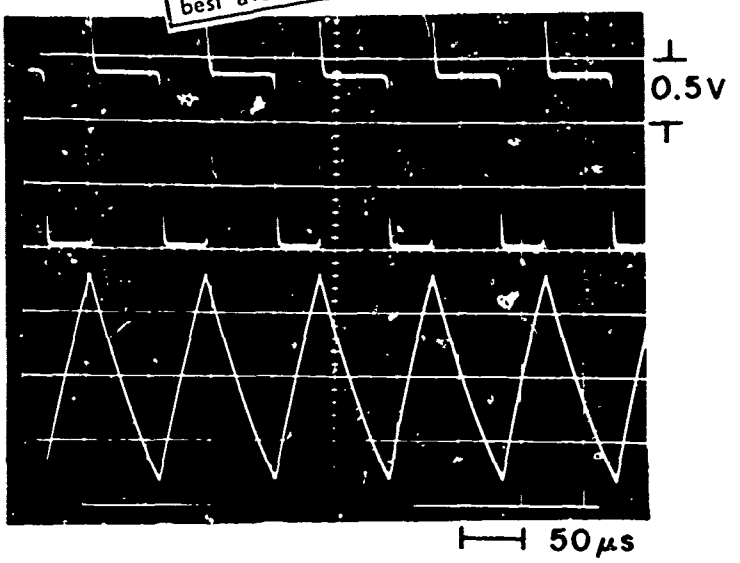



Figure 11. Voltage Waveforms for Integrated 11.1-kHz Square-Wave Oscillator with 0.0027-$\mu$F Thin-Film Capacitor.

Upper trace — square-wave output
Lower trace — voltage across capacitor

(1) Beginning with the passivated silicon wafer containing contact windows to the transistors, resistors, and cross-unders, deposit a 1-$\mu$m-thick aluminum film by evaporation from a tungsten filament.

(2) Remove aluminum from the three capacitor areas and delineate the interconnection pattern, using a phosphoric acid etch solution.

(3) Heat the wafer to sinter the aluminum to the silicon in the contact windows. The reason for removing the aluminum from the capacitor areas in step (2) is to prevent the formation of a roughened base electrode and possible degradation of the capacitors as a result of the sintering.

(4) Deposit a second aluminum film.

(5) Remove the aluminum from the perimeter of the capacitor base electrode area, leaving an interconnection to the remainder of the circuit. Figure 12 shows the capacitor areas at the conclusion of this step. The transistors are short-circuited by the aluminum film to protect them from damage during the NiO sputtering (Step (7)).

(6) Thermally oxidize the aluminum to form a thin aluminum oxide film.

(7) Deposit a nickel oxide film by sputtering.

(8) Remove the nickel oxide, by etching in 85 percent sulfuric acid, from all areas but the capacitors. The NiO film is allowed to overlap the base electrode on all sides.

(9) Delineate the interconnection pattern in the exposed aluminum film.

(10) Deposit a third aluminum film.

(11) Etch the aluminum to delineate the top electrodes of the capacitors and the final interconnection pattern. A completed circuit is shown in Figure 13. An enlarged view of the completed capacitors is shown in Figure 14.

The ability to prepare circuits that operate at or near the design frequency of 10 kHz demonstrated the feasibility of incorporating the 10 $\mu F/in^2$ capacitors in a practical monolithic circuit. However, several factors contributed to a low yield. The use of three aluminum deposition steps resulted in thick conductors that often showed discontinuities. There were also poor aluminum-to-aluminum contacts as a result of the oxidation in Step (6). Because the chip was not designed specifically for this circuit, there were capacitor failures due to the presence of steps in the silicon surface.

## 3.2 Monolithic 1-kHz Oscillator

The goal of the most recent phase of the program was to improve the fabrication process and to provide a circuit that satisfies a specific ECOM need. The circuit selected was a square-wave oscillator that operates in the range between 0.9 and 1.2 kHz and that provides a peak output of at least 7 volts when a 9-volt power supply is used.

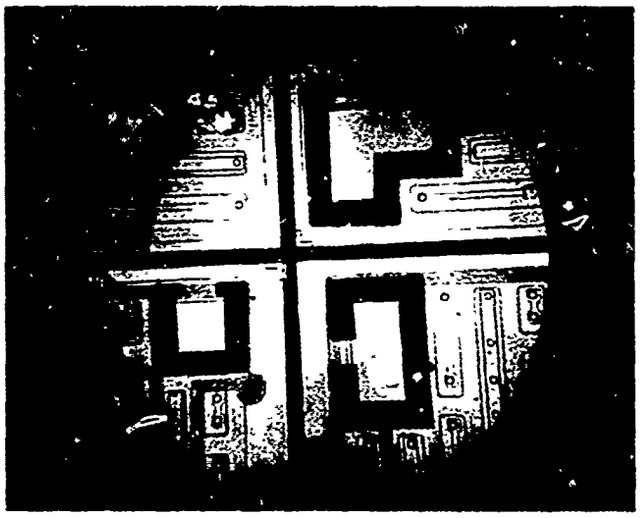


Figure 12. 10-kHz Oscillator Wafer after Step (5) of the Fabrication Process, Showing Outlines of the Three Capacitor Areas.

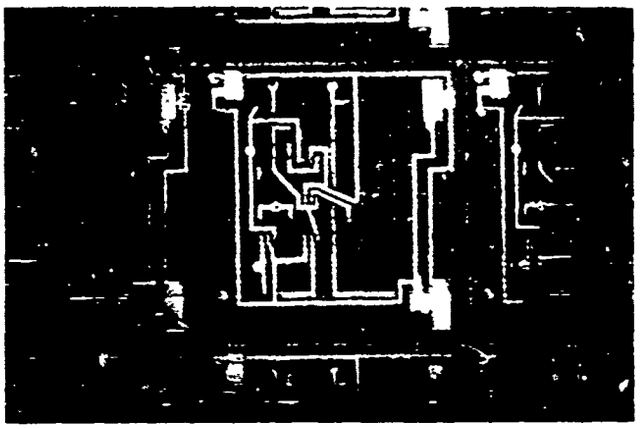


Figure 13. Completed integrated 10-kHz Oscillator.

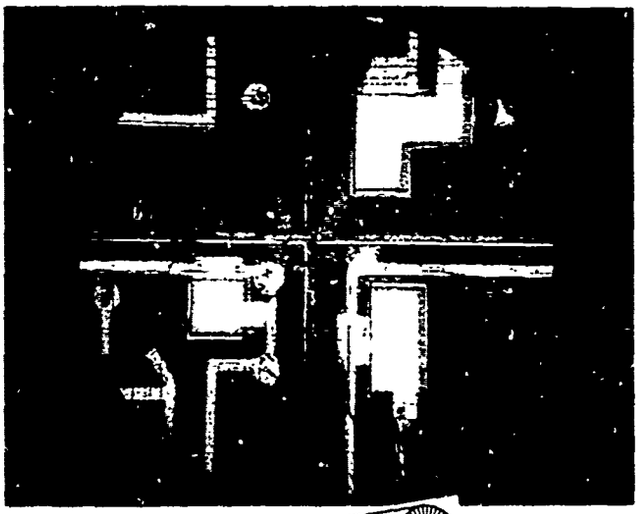


Figure 14. Enlarged View of Capacitors on 10-kHz Oscillator Circuit.

### 3.2.1 Circuit Design

The circuit selected to meet the required performance is the free-running multivibrator shown in the schematic of Figure 15. The half period of oscillation is determined by the time required to charge each capacitor to voltage $V_1$, through the composite pnp-npn current sources. The frequency is inversely proportional to $V_1$ and to the capacitance, and is directly proportional to the charging current supplied by the current sources. This current is in turn an inverse function of the resistance $R^*$. The component values were chosen to provide the proper frequency for $V_1 < 5$ volts and $R^* = 25,000$ ohms. The output circuit is independent of the oscillator, so that the output voltage swing is effectively zero to $V_2$, where $V_2$ may be as high as 25 volts. The voltage waveforms shown in Figure 16 were obtained from a breadboard version of the circuit; they were measured at the numbered points in the schematic. For the generation of a symmetrical square wave with a nominal frequency of 1 kHz, the required capacitance values are $C_1 = 0.0010\ \mu F$ and $C_2 = 0.0018\ \mu F$.

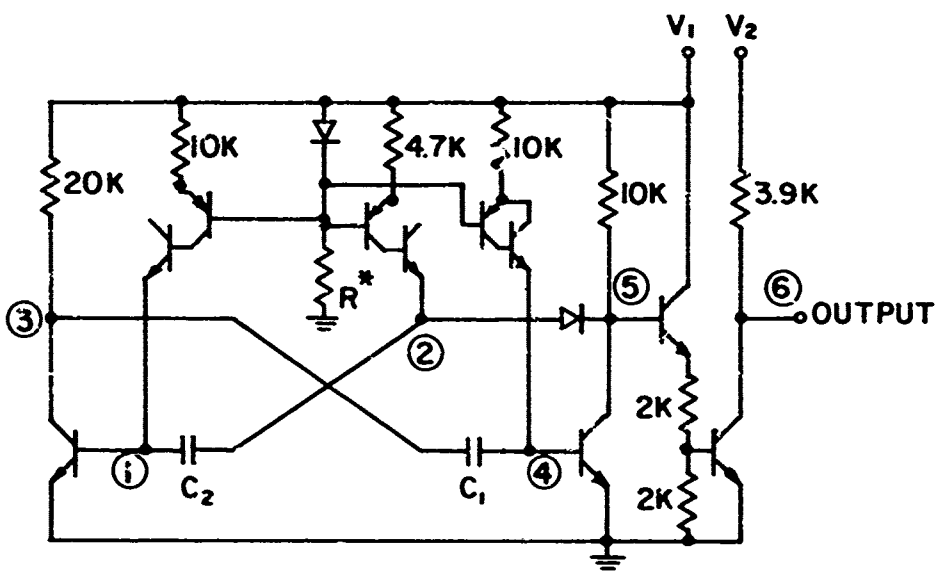



Figure 15. Schematic of Integrated 1-kHz Oscillator.

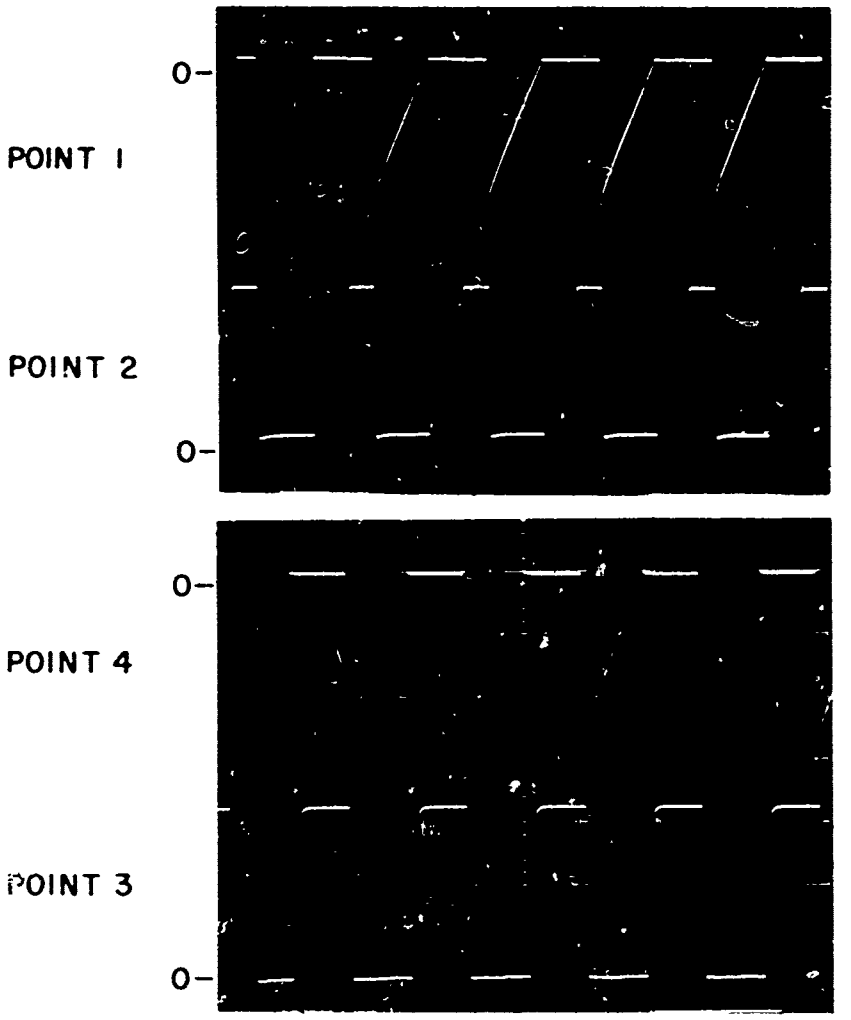



Figure 16. Voltage Waveforms at Indicated Points in Figure 15.

$V_1 = V_2 = 5$ volts

$R^* = 10$ kilohms

Vertical scale — 2 volts/div.

Horizontal scale — 0.5 ms/div.

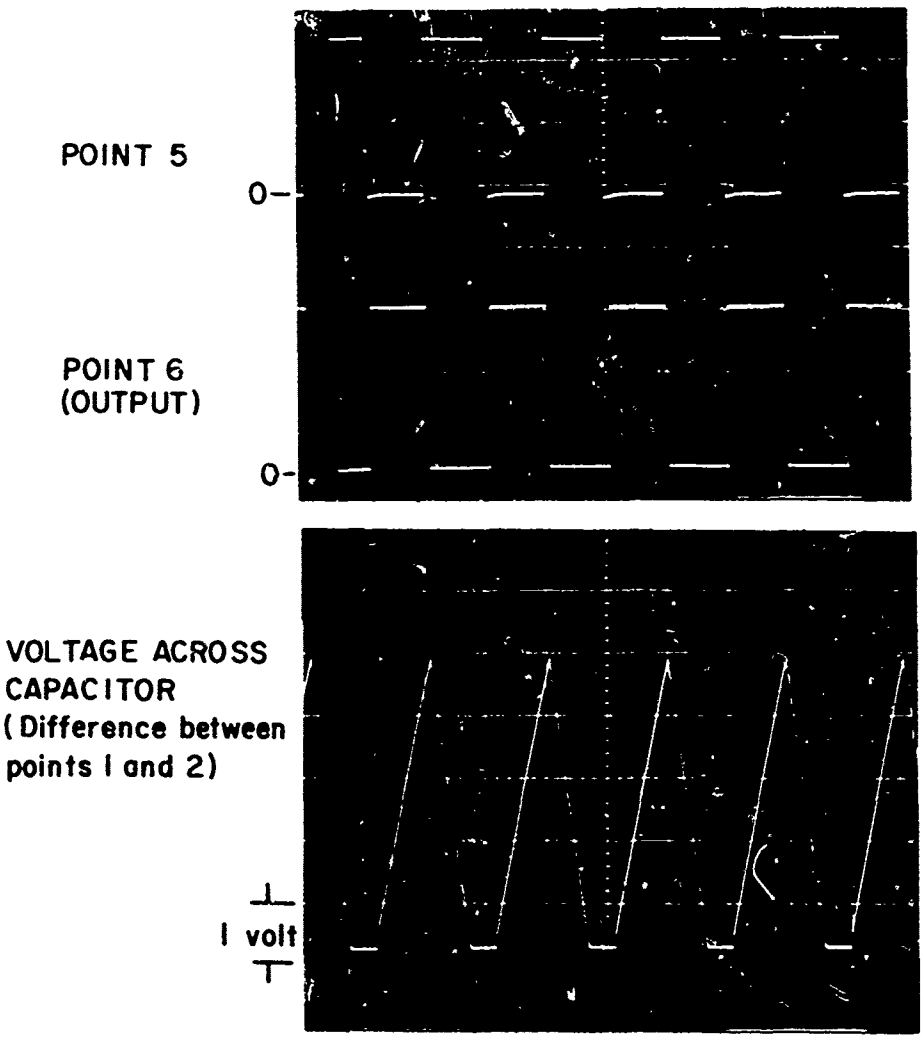



Figure 16. (Continued)

### 3.2.2 Circuit Fabrication

Since the utility of the capacitor fabrication process would be severely restricted if its use required changes in the silicon wafer processing, it was decided that only conventional processing steps would be employed up to the point of the capacitor formation. A 60 mil x 70 mil chip was designed which contains lateral pnp transistors and dielectric isolation moats for the components. The processing of circuits of this type is done routinely in our Laboratories. In its final form, ready for the capacitor fabrication, the wafer was $SiO_2$-passivated with open contact windows to the substrate. It was subjected to an annealing step at 1050°C in argon, to adjust the beta of the npn transistors to approximately 150. This value was determined by connecting external capacitors to the circuit and measuring the oscillation frequency as a function of the transistor gain. The following linear approximation was derived:

$$f(\text{in kHz}) = 1.714 - 5.938 \times 10^{-3} \beta$$

In the following description of the capacitor fabrication and completion of the oscillator circuit, the discussion of each step is accompanied by a photograph (47 x) of the photolithographic masks used in that step.

Step 1 — Deposit a 1-$\mu$m aluminum film, delineate interconnection pattern and capacitor base electrodes (Figure 17(a)) using Shipley positive photoresist. Sinter to form ohmic contacts to the silicon.

Step 2 — Deposit a 0.3-$\mu$m $SiO_2$ film by low-temperature oxidation of silane. Remove from the capacitor areas (Figure 17(b)) to expose the base electrodes, using Dynachem CRM 5000 negative photoresist. This step protects the remainder of the aluminum pattern throughout the rest of the process. It circumvents the difficulties previously encountered by the buildup of aluminum during successive depositions.

Step 3 — Deposit a second aluminum layer, 0.3-$\mu$m thick, and use the same mask (Figure 17(b)) to delineate the base electrodes. The purpose of this step is to provide a smoother aluminum surface for formation

of the capacitor. The original aluminum layer was roughened by the sintering step and by the etching of the $SiO_2$ window. Furthermore, if traces of $SiO_2$ remain after the etching, they are covered by the second aluminization.

Step 4 — Oxidize the aluminum at 500°C in dry oxygen for two minutes. The interconnection pattern, which is covered by the $SiO_2$ layer, is unaffected by this oxidation.

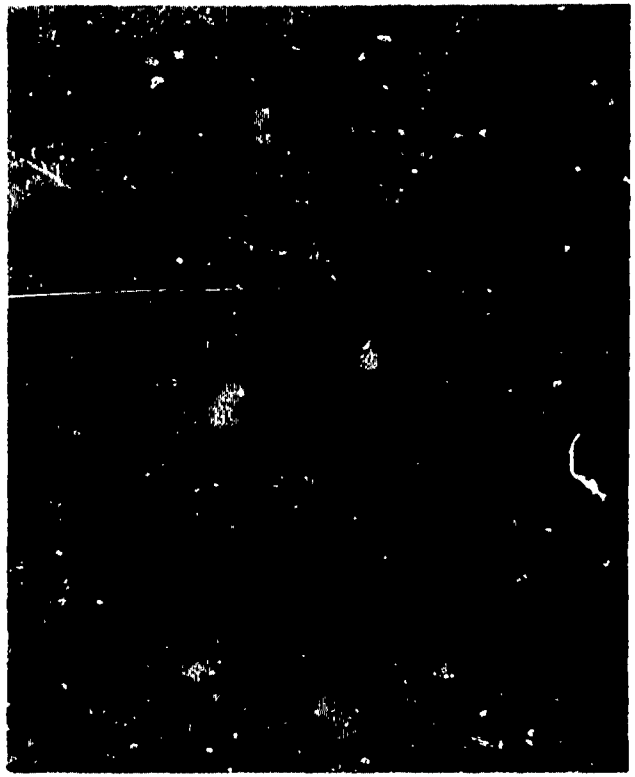
Step 5 — Deposit a nickel oxide film by dc sputtering of nickel in oxygen. Cathode potential - 2.5 kV; $O_2$ pressure - 50 millitorr; sputtering time - 15 minutes. Remove the NiO from all areas but the capacitor (Figure 17(c)), using the Dynachem photoresist and hot 85 percent sulfuric acid as the etching reagent. The area of the remaining NiO film is slightly greater than that of the base electrode.

Step 6 — Remove the protective $SiO_2$ layer from the contact pads and from a small part of the interconnection pattern to permit the top electrode to connect into the circuit (Figure 17(d)).

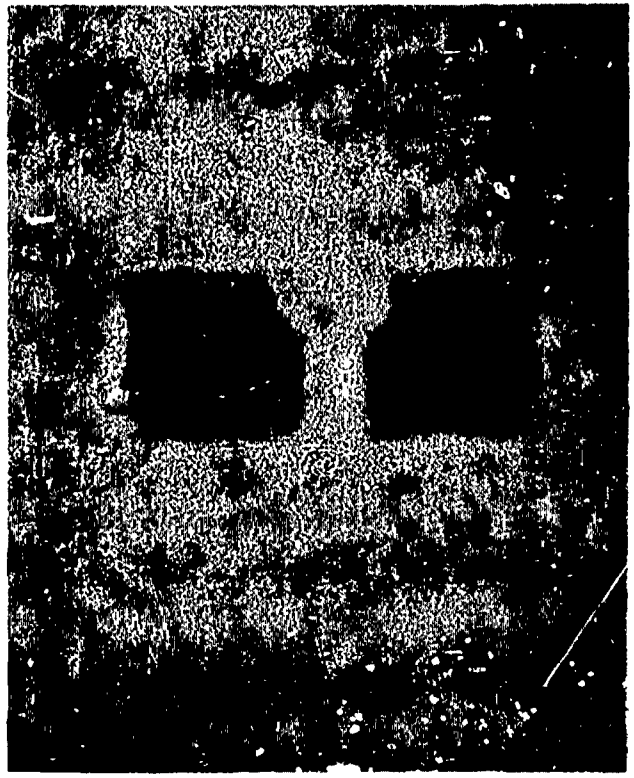
Step 7 — Deposit a 0.4-$\mu$m aluminum film and delineate to form the top electrode of the capacitors and to reinforce the contact pads (Figure 17(e)). This step determines the areas of the capacitors.

A portion of a completed wafer is shown in Figure 18, and a more detailed view of a single circuit is seen in Figure 19. The area occupied by the capacitors is comparable with that required for the transistors on the 60 mil x 70 mil chip. The effectiveness of the $SiO_2$ masking process is shown by the fact that the circuits operate immediately upon contacting them with probes; no manipulations are required to break through insulating films between aluminum layers. The insulating $SiO_2$ film also protects the transistors from developing leakage as a result of the sputtering process.

The chips were mounted on 10-pin TO-5 headers, as shown in Figure 20. Although low-melting solders, such as 63 Sn-37 Pb, have been used successfully for chip bonding without damaging the capacitors, epoxy cement was used in most cases for



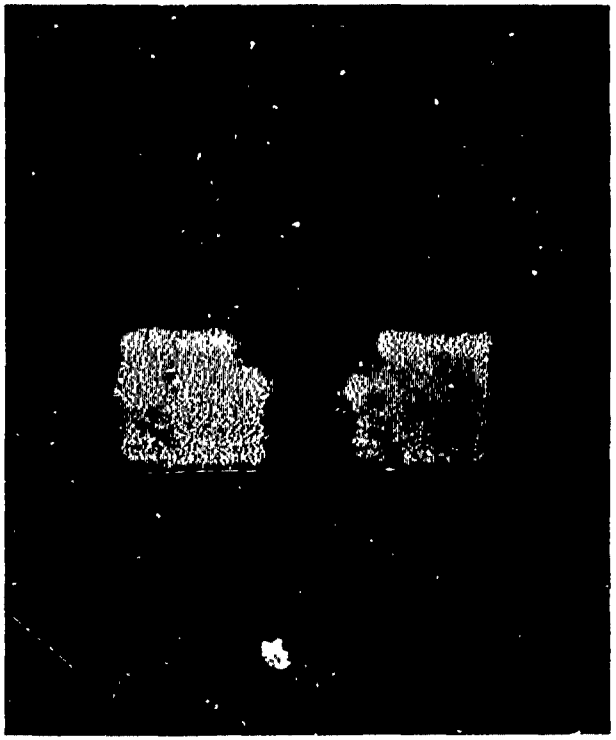




(a) ALUMINUM INTERCONNECTION PATTERN AND CAPACITOR BASE ELECTRODES

(b) OPENINGS IN $SiO_2$ LAYER FOR CAPACITOR BASE ELECTRODES

Figure 17. Sequence of Photomasks Used in Fabrication of 1-kHz Oscillator (47 x Magnification)



(c) NICKEL OXIDE FILM



(d) OPENINGS IN $SiO_2$ LAYER FOR TOP ELECTRODE CONNECTION AND CONTACT PADS

Figure 17. (Continued)

(e) FINAL ALUMINUM PATTERN INCLUDING CAPACITOR TOP ELECTRODES

Figure 17. (Continued)

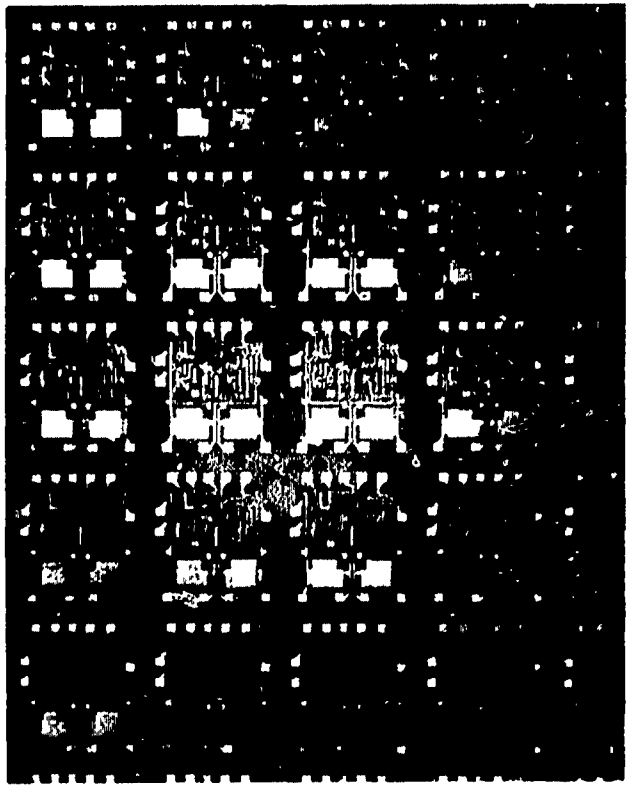


Figure 18. Wafer Containing Completed 1-kHz Oscillator Chips.



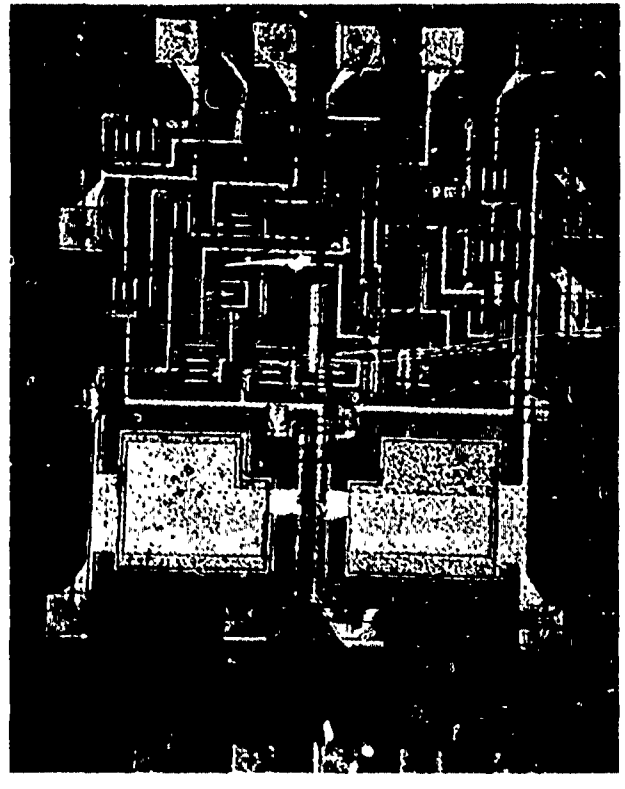


Figure 19. Details of a Single Oscillator Chip.



Figure 20. Oscillator Chip Mounted on 10-Pin TO-5 Header.

simplicity. The nonconductive epoxy can be used because the silicon substrate is already isolated by $SiO_2$ moats from the circuit components, and therefore is not a part of the circuit. The pin connections, numbering clockwise from the tab in a top view of the case, are:

1 - top electrode of $C_2$
2 - top electrode of $C_1$
3 - base electrode of $C_1$
4 - no connection
5 - ground
6 - oscillator supply $V_1$
7 - output supply $V_2$

8 - output

9 - no connection

10 - base electrode of $C_2$

The connections to the capacitors are made for convenience of testing. The only pins necessary for operation of the circuit are 5, 6, 7, and 8. There are 12 contact pads on the chip (the large squares around the periphery of Figure 17(e)). Beginning at the top left of Figure 17(e) and moving clockwise, the pads connect to the following parts of the circuit:

Ground (pin 5 and header)

High side of R* (no pin). For test purposes.

$V_1$ (pin 6)

$V_2$ (pin 7)

Output (pin 8)

Ground (to header)

$C_2$ base electrode (pin 10). For test purposes.

$C_2$ top electrode (pin 1). For test purposes.

$C_1$ top electrode (pin 2). For test purposes.

$C_1$ base electrode (pin 3). For test purposes.

20 kilohm tap on R* (no pin). For optional connection to ground.

Low side of R* (to header)

### 3.2.3 Circuit Performance

The 1-kHz oscillator circuits were initially fabricated by the process described in Section 3.1, in which the aluminum-silicon contacts were exposed during sputtering and which required thermal oxidation of the entire metallization pattern and multiple aluminum depositions. The deposition of capacitors on these circuits was refined to the point where an 80 percent yield of capacitors with 10 to 11 $pF/mil^2$ was obtained. However, very few operating circuits were obtained because of faulty metallizations and poor aluminum-silicon contacts. Some circuits operated under illumination, which generated sufficient carriers to overcome the aluminum-silicon barriers.

The $SiO_2$ masking procedure described in Section 3.2.2 was successful in overcoming many of the losses resulting from metallization and contact imperfections. The most recent wafers fabricated by this technique contained 60 to 80 percent of operating oscillator chips. However, the spread in capacitor values was larger than obtained in the earlier process as a result of the greater complexity in the capacitor deposition (Steps 2 and 3) required by the $SiO_2$ mask technique. The range of output frequencies was between 0.9 and 5 kHz. As an example of the results of the $SiO_2$ masking process, one wafer showed the following performance:

- 26 of the 30 chips operating with outboarded capacitors before deposition of the thin-film capacitors.
- 16 of the 26 chips operating on the first probing after capacitor deposition.
- 6 of the 16 chips operating in the frequency range of 0.9 to 1.2 kHz on probe test.

Figure 21 shows the output waveform and capacitor voltage for a completed chip. The frequency was 1.196 kHz for an oscillator supply voltage of 2.6 volts. However, those circuits that oscillated initially in or near the 0.9 to 1.2 kHz range changed their characteristics in less than 24 hours. There was a decrease in capacitance and a corresponding increase in the output frequency. Most of the circuits now exhibit an output frequency between 2 and 3 kHz when operated with $V_1 = 2.5$ volts. Representative examples of the capacitance decrease are shown in Table 1. The design values were $C_1 = 1.0$ nF and $C_2 = 1.8$ nF.



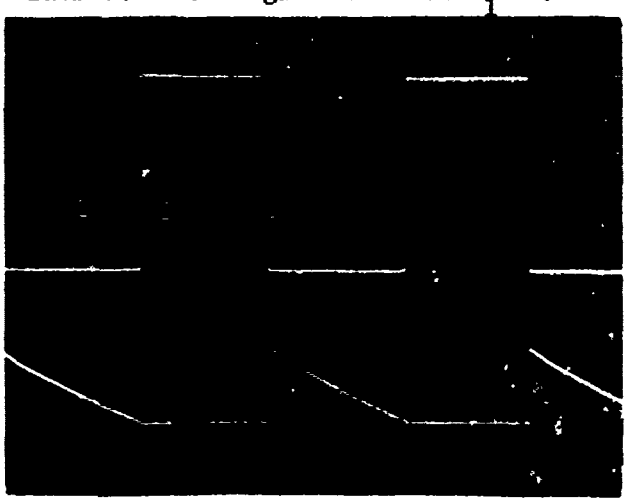



Figure 21. 1-kHz Oscillator Waveforms.
Upper trace — 15 volt, 1.196-kHz, square-wave output (5 volts/div.); Lower trace - voltage across capacitor (2 volts/div.)

TABLE 1

SHORT-TERM AGING OF CAPACITORS ON SAMPLE 2ISO-11C

| Chip No. | | Initial Values | | Values after 7 days | | Percent Decrease in C |
|---|---|---|---|---|---|---|
| | | C (nF) | D | C (nF) | D | |
| 12 | $C_1$ | 1.059 | 0.040 | 0.552 | 0.197 | 48 |
| | $C_2$ | 1.801 | 0.024 | 1.445 | 0.103 | 20 |
| 22 | $C_1$ | 1.093 | 0.027 | 0.758 | 0.168 | 31 |
| | $C_2$ | 1.806 | 0.023 | 1.320 | 0.121 | 27 |
| 23 | $C_1$ | 1.066 | 0.032 | 0.673 | 0.186 | 37 |
| | $C_2$ | 1.787 | 0.023 | 1.462 | 0.097 | 18 |

This degradation of the capacitor values is a new phenomenon that is inconsistent with the vast majority of our experimental results. More typical are the life test results on sample capacitors (Section 2.4) that showed a change of less than one percent after 10,000 hours of operation. Moreover, capacitors in complete circuits made earlier without the $SiO_2$ masking process changed by less than one percent after storage for periods ranging from 30 to 90 days.

A tentative conclusion concerning the cause of the degradation can be drawn from data such as those given in Table 1. The two significant points are that the relative decrease in capacitance is generally smaller in $C_2$, which occupies the larger area of the two capacitors on the chip, and that the decrease in capacitance is accompanied by an increase in dissipation factor. The combination of a decrease in the equivalent series capacitance and an increase in the dissipation factor must be attributed to an increased series resistance over part of the capacitor area. If the increased dissipation were the result of losses within the $Al_2O_3$ dielectric, the equivalent series capacitance would

increase. The proposed explanation is consistent with the observed relationship between capacitor area and percent decrease in capacitance. If the source of the degradation is, for example, a lifting of the top electrode that begins at the edges and propagates inward at a constant linear rate, the change in capacitance will be an inverse function of the area. This relationship may be demonstrated for a circular area of radius r, where the capacitance C is proportional to the area

$$C = k\pi r^2$$

The relative change in capacitance for a change, dr, in radius is

$$\frac{dC}{C} = \frac{2k\pi r\, dr}{k\pi r^2} = \frac{2dr}{r}$$

Therefore, if dr per unit time is constant for all capacitors, the relative change in C is less for larger areas.

The true cause of the capacitor degradation has not been identified. Although the effect has been observed only in the latest circuits, which were fabricated with the use of a deposited $SiO_2$ mask to protect the transistors and the metallization, there is insufficient information to permit the conclusion that there is a cause inherent in the masking process. Since other samples made with the $SiO_2$ mask showed little or no downward drift in capacitance, the problem is more likely an isolated processing defect that should have no long-range impact on the applicability of the fabrication process.

The 20 oscillator circuits which were delivered under this contract are described in Table 2. The design values of capacitance are $C_1 = 1.0$ nF and $C_2 = 1.8$ nF. The two circuits from wafer 10C have the proper capacitance values but have other circuit defects. In the case of sample 10C-52, the defect is apparently the presence of barriers at one or more aluminum-silicon contacts, which are overcome by using low-level illumination to generate carriers.

TABLE 2

CHARACTERISTICS OF INTEGRATED SQUARE-WAVE OSCILLATORS

| Sample Number | Frequency at $V_1$=2.5 volts (kHz) | Symmetry Factor* | $C_1$ (nF) | $D_1$ | $C_2$ (nF) | $D_2$ | Encapsulation | Remarks |
|---|---|---|---|---|---|---|---|---|
| 7B-12 | 2.48 | 0.56 | 0.510 | 0.032 | 0.657 | 0.033 | Sealed in $N_2$ | |
| 7B-21 | 2.40 | 0.67 | 0.502 | 0.032 | 0.793 | 0.034 | " | |
| 7B-23 | 2.87 | 0.67 | | | 0.594 | 0.034 | " | $C_1$ test contact open. |
| 7B-24 | 3.12 | 0.79 | 0.346 | 0.030 | 0.580 | 0.030 | " | |
| 7B-32 | 2.89 | 0.70 | 0.377 | 0.033 | 0.593 | 0.033 | " | |
| 7B-35 | 2.95 | 0.75 | 0.413 | 0.032 | 0.635 | 0.031 | " | |
| 7B-51 | 2.89 | 0.73 | 0.419 | 0.024 | 0.648 | 0.033 | " | |
| 7B-53 | 3.09 | 0.64 | 0.400 | 0.034 | 0.596 | 0.031 | " | |
| 7B-62 | 2.79 | 0.70 | 0.430 | 0.031 | 0.668 | 0.031 | " | |
| 7B-63 | 2.77 | 0.70 | 0.428 | 0.031 | 0.675 | 0.031 | " | |
| 7B-65 | 3.10 | 0.75 | | | 0.705 | 0.030 | Cap removable | Window in cap. $C_1$ test contact open. |
| 11C-32 | 3.06 | 1.0 | 0.324 | 0.045 | 0.643 | 0.122 | " | |
| 10C-43 | 2.46 | 0.32 | 1.142 | 0.032 | 1.877 | 0.024 | " | |
| 10C-52 | 0.99 | 0.85 | 1.195 | 0.019 | 1.966 | 0.017 | " | Window in cap. Output measured under illumination. |
| 2 | 3.62 | | | | | | " | |
| 5 | 2.86 | | | | | | " | |
| 6 | 4.49 | | | | | | " | |
| 11 | 3.40 | | | | | | " | |
| 12 | 3.66 | | | | | | " | |
| 13 | 4.55 | | | | | | " | |

*Symmetry factor is the ratio of the ON-time to the OFF-time of an output cycle. It is 1.0 for a true square wave.

Also delivered were two wafers containing test capacitors, to demonstrate the ability to achieve the design value under the appropriate conditions. The capacitance values are given in Tables 3 and 4. Sample DISO2-13 contains 132 capacitors, nominally 1.0 nF on passivated silicon. Sample 2DISO-1 was prepared on passivated silicon with the photoresist masks used for the 1-kHz oscillator, but with equal-area 1.0 nF capacitors.

TABLE 3

CHARACTERISTICS OF THIN-FILM CAPACITORS ON WAFER DISO2-13
(Random Sample of 132 Elements, Each 110 $Mil^2$)

| Element Number | C (nF) | D |
|---|---|---|
| 1-8 | 0.865 | 0.029 |
| 1-12 | 0.883 | 0.029 |
| 2-9 | 0.886 | 0.029 |
| 2-15 | 0.882 | 0.033 |
| 3-7 | 0.875 | 0.029 |
| 3-11 | 0.884 | 0.030 |
| 3-14 | 0.903 | 0.031 |
| 4-10 | 0.894 | 0.025 |
| 4-13 | 0.882 | 0.030 |
| 5-8 | 0.893 | 0.030 |
| 5-12 | 0.893 | 0.030 |
| 6-9 | 0.897 | 0.029 |
| 6-14 | 0.899 | 0.031 |
| 7-7 | 0.905 | 0.030 |
| 7-11 | 0.896 | 0.029 |
| 7-15 | 0.909 | 0.030 |
| 8-10 | 0.908 | 0.030 |
| 9-8 | 0.903 | 0.029 |
| 9-12 | 0.904 | 0.030 |
| 10-5 | 0.869 | 0.028 |
| 10-9 | 0.912 | 0.030 |
| 10-13 | 0.910 | 0.030 |
| 11-7 | 0.915 | 0.030 |
| 11-11 | 0.919 | 0.030 |
| 11-14 | 0.899 | 0.029 |
| 12-6 | 0.903 | 0.030 |
| 12-9 | 0.912 | 0.030 |
| 12-10 | 0.900 | 0.030 |
| 12-16 | 0.934 | 0.030 |

TABLE 4

CHARACTERISTICS OF 110 MIL$^2$ THIN-FILM CAPACITORS ON WAFER 2DISO-1

| Chip Number | $C_1$ (nF) | $D_1$ | $C_2$ (nF) | $D_2$ |
|---|---|---|---|---|
| 11 | short | | 1.169 | 0.015 |
| 12 | 1.137 | 0.017 | 1.152 | 0.015 |
| 13 | 1.065 | 0.133 | 1.075 | 0.016 |
| 14 | 1.027 | 0.014 | 1.063 | 0.014 |
| 15 | short | | open | |
| 21 | 1.100 | 0.016 | 1.124 | 0.016 |
| 22 | 1.094 | 0.019 | 1.104 | 0.016 |
| 23 | 1.049 | 0.018 | 1.068 | 0.015 |
| 24 | 1.122 | 0.016 | 1.146 | 0.014 |
| 25 | 1.051 | 0.017 | 1.119 | 0.016 |
| 31 | 1.000 | 0.014 | 1.142 | 0.015 |
| 32 | 1.074 | 0.017 | 0.934 | 0.093 |
| 33 | 1.120 | 0.015 | 1.155 | 0.014 |
| 34 | 1.050 | 0.021 | 1.026 | 0.017 |
| 35 | 1.109 | 0.014 | 1.125 | 0.017 |
| 41 | open | | 1.097 | 0.014 |
| 42 | 1.000 | 0.014 | 1.066 | 0.013 |
| 43 | open | | 1.053 | 0.016 |
| 44 | open | | 1.125 | 0.015 |
| 45 | open | | open | |
| 51 | 1.118 | 0.016 | 1.110 | 0.015 |
| 52 | 1.054 | 0.019 | 1.073 | 0.019 |
| 53 | 1.123 | 0.016 | 1.096 | 0.015 |
| 54 | 1.083 | 0.020 | 1.112 | 0.019 |
| 55 | 1.121 | 0.025 | 1.125 | 0.015 |
| 61 | open | | open | |
| 62 | open | | 0.868 | 0.033 |
| 63 | 1.095 | 0.017 | 1.089 | 0.020 |
| 64 | 1.048 | 0.019 | 0.964 | 0.020 |
| 65 | 1.147 | 0.050 | short | |

## 4. CONCLUSIONS AND RECOMMENDATIONS

The ability to fabricate a high yield of 10 $\mu F/in^2$ thin-film capacitors on the surface of a silicon-integrated circuit has been demonstrated. The capacitor deposition method has been adapted to the fabrication in high yield of an integrated low-frequency square-wave oscillator. However, the modifications required in the capacitor processing for the oscillators caused a reduction in the specific capacitance in most cases to values between 3 and 5 $\mu F/in^2$. Consequently, most of the circuits have an output frequency between 2 and 3.5 kHz, rather than in the design range of 0.9 to 1.2 kHz.

The low values of capacitance probably arise from the condition of the aluminum base electrode after Steps 2 and 3 of the fabrication process (Section 3.2.2). It is at this point that the circuit fabrication departs from the earlier process that gave a high yield of 10 $\mu F/in^2$ capacitors. The surface of the aluminum base electrode is influenced by the sintering process used to form ohmic contacts to the silicon, by the deposition of $SiO_2$, and by the removal of the $SiO_2$ layer by an HF etch. Although Step 3, the deposition of a second aluminum layer over the initial one, was included to provide a smoother surface for the capacitor formation, this surface has not been characterized, and is likely to be rougher and less reproducible than one which has not been subjected to this sequence of steps.

The $SiO_2$ masking procedure is extremely effective in increasing the yield of working circuits; it should therefore be retained. The following procedure is proposed for providing more reliabile capacitor base electrodes. The starting point is the same as in Section 3.2.2.

Step 1 — Deposit an aluminum film, delineate the interconnection pattern without the capacitor base electrodes, and sinter to form ohmic contacts to the silicon.

Step 2 — Deposit a $SiO_2$ film, and remove only to form contact windows for the capacitor base electrodes.

Step 3 — Deposit aluminum and delineate the base electrodes on the surface of the deposited $SiO_2$, as well as their connections through the contact windows to the interconnection pattern.

Step 4 — Thermally oxidize the aluminum.

Step 5 — Deposit NiO by sputtering and remove from all areas but the base electrode.

Step 6 — Remove the $SiO_2$ layer from the contact pads and from regions of the interconnection pattern where the capacitor top electrode will be connected.

Step 7 — Deposit an aluminum film and delineate to form the top electrodes and their connection to the rest of the circuit.

In this method the capacitors are formed on a freshly deposited aluminum film. They should then be comparable with the earlier ones, and it should therefore be possible to obtain a high yield of operating circuits that contain 10 $\mu F/in^2$ thin-film capacitors.

## 5. REFERENCES


1. M. S. Wasserman and A. E. Feuersanger, "High Capacitance Thin Film Structures," Final Report on Contract DAAB07-69-C-0194 (July 1970).

2. M. S. Wasserman and A. E. Feuersanger, "High Capacitance Thin Film Structures," Final Report on Contract DAAB07-70-C-0169 (September 1971).